**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) A receiver signal strength indication circuit receiving a discretely controlled amplified signal from an amplifying means (A1-A4), the circuit comprising:

narrow filter means coupled to an output of the discretely controlled amplifying means (A1-A4), said narrow filter means providing a limited spectrum of the input signal;

logarithmic detector means for receiving and logarithmically amplifying an output of the narrow filter~~; and~~

analog-to-digital (ADC) means for converting the output of the logarithmic detector to a digital receiver signal strength indication~~, wherein the ADC means is configured to store an amplification setting of the discretely controlled amplifying means relative to a first radio-frequency (RF) input level and the digital receiver signal strength indication in a memory device, wherein the stored amplification setting is configured to serve as a reference to tune the circuit for a subsequent RF input level.~~; and

memory means to store an amplification setting of the discretely controlled amplifying means relative to a first radio-frequency (RF) input level and the digital receiver signal strength indication, wherein the stored amplification setting is configured to serve as a reference to tune the circuit for a subsequent RF input level.

2. (canceled)

3. (previously presented) An integrated tuner comprising a receiver signal strength indication circuit as claimed in claim 1, wherein the amplifying means (A1-A4, SF1, SF2, M) include selectivity filtering means (SF1, SF2) connected between the discretely controlled amplifying means and the logarithmic detector means.

4. (previously presented) An integrated tuner comprising a receiver signal strength indication circuit as claimed in claim 1, wherein the amplifying means (A1-A4, SF1, SF2) include a mixer (M).

5. (new) The receiver signal strength indication circuit of claim 1, wherein the receiver signal strength indication circuit comprises an integrated tuner, wherein the memory means is placed on the receiver signal strength indication circuit separate from the integrated tuner.

6. (new) The receiver signal strength indication circuit of claim 1, wherein the receiver signal strength indication circuit comprises an integrated tuner, wherein the memory means is integrated into the integrated tuner.